What is claimed is:

1. An information processing system including a processor, a hardware timer built in said processor or provided outside said processor, and a clock pulse generator for supplying a clock to both of said processor and said hardware timer,

wherein said hardware timer measures a processing time between starting and ending points of an application task;

wherein said application task is divided into a plurality of processing units;

wherein said processor compares a time required to process a predetermined one of said plurality of processing units of said application task with the worst case execution time of said plurality of processing units and changes the clock frequency output from said clock pulse generator according to a result of said comparison; and

wherein said processor counts the number of application tasks set in the ready state when a different application task started up by an interruption during the former application task processing occupies the computing resource of said processor so as to enable said ready state watching task to raise both of said clock frequency and said source voltage when there is any application task set in the ready state other than said different application task to

be executed and lower both of said clock frequency and said source voltage when there is no task set in the ready state.

2. The information processing system according to claim 1,

wherein, if said processor is notified of existence of a different application task set in the ready state other than said application task when executing said application task, said application task compares the virtual worst case execution time that is earlier than said worst case execution time with said time required to process said predetermined processing unit.

3. The information processing system according to claim 2,

wherein said processor lowers both of said clock frequency and said source voltage used for executing said current active application task if said difference between said worst case execution time or said virtual worst case execution time and said time required to process said predetermined processing unit is greater than a predetermined time and raise both of said clock frequency and said source voltage if said time difference is less than said predetermined time as a result of comparison between said worst case execution time or said virtual worst case execution time and said time required to process said predetermined processing unit.

4. The information processing system according to claim 1,

wherein said processor, if it inquires said ready state watching task and knows existence of any ready state application task other than said different application task, enables said different application task to measure the preset virtual worst case execution time that is earlier than said worst case execution time and if it knows no existence of such a ready state task, enables said different task to measure how much time to spare is left according to the original worst case execution time.

5. The information processing system according to claim 4,

wherein said processor lowers both of said clock frequency and said source voltage used to execute said current active task when said time to spare measured according to said worst case execution time or said virtual worst case execution time is greater than a predetermined time and raise both of said clock frequency and said source voltage if said execution time is less than said predetermined space time.

6. The information processing system according to claim 2,

wherein said processor decides how much said worst case execution time should be set earlier in said virtual

worst case execution time according to the number of ready state application tasks.

7. The information processing system according to claim 4,

wherein said processor counts the number of ready state application tasks in response to an inquiry from said different application task and issues a system call to said different application task to notify the number of said ready state application tasks or existence/absence of them.

8. The information processing system according to claim 4,

wherein said processor operates under the control of an operating system.

9. An information processing system including a processor, a timer, a clock generator, and a clock voltage supply circuit,

wherein said timer measures an execution time of an application task to be executed by said processor;

wherein said application task is divided into a plurality of processing units;

wherein said information processing system manages the number of ready state application tasks;

wherein said information processing system manages the worst case execution time in which processing of each of said plurality of processing units should be completed

if the number of ready state application tasks is less than a predetermined value and manages the virtual worst case execution time that is shorter than said worst case execution time for each of said plurality of processing units if the number of ready state application tasks is greater than said predetermined value when enabling said processor to execute said first application task.

10. The information processing system according to claim 9,

wherein said information processing system has a first power mode and a second power mode that consumes less power than said first power mode;

wherein said information processing system, when said first application task ends a predetermined processing unit, compares the execution time of said predetermined processing unit measured by said timer with said worst case execution time or said virtual worst case execution time corresponding to said predetermined processing unit; and

wherein said information processing system operates in said second power mode if the difference between said worst case execution time or said virtual worst case execution time corresponding to said predetermined processing unit and the execution time of said predetermined processing unit is greater than a predetermined time and

operates in said first power mode if said difference is less than said predetermined time.

11. The information processing system according to claim 10,

wherein the clock frequency of said processor is lower in said second power mode than in said first power mode; and

wherein the source voltage of said processor is lower in said second power mode than in said first power mode.

12. The information processing system according to claim 11,

wherein said information processing system that operates in said second power mode, when said first application task ends a predetermined processing unit, goes into said first power mode if the number of ready state application tasks is greater than a predetermined value.

13. An operating system for controlling an information processing system that includes a processor and a timer, said system comprising the steps of:

dividing an application task executed by said processor into a plurality of processing units and managing the number of ready state application tasks; and

managing the worst case execution time in which each of said plurality of processing units should be completed if the number of ready state application tasks is less than a predetermined value and managing the virtual worst case

execution time that is shorter than said worst execution time corresponding to each of said plurality of processing units if the number of ready state application tasks is greater than said predetermined value when enabling said processor to execute a first application task.

14. The information processing system according to claim 13,

wherein said information processing system has a first power mode and a second power mode that consumes less power than said first power mode;

wherein said operating system compares the execution time of said predetermined processing unit measured by said timer with said worst case execution time or said virtual worst case execution time corresponding to said predetermined processing unit when said first application task ends a predetermined processing unit, then operates said apparatus in said second power mode if the difference between said worst case execution time or said virtual worst case execution time corresponding to said predetermined processing unit and the execution time of said predetermined processing unit is greater than a predetermined time and operates said apparatus in said first power mode if said difference is less than said predetermined time.

15. The information processing system according to claim 14,

wherein said operating system shifts said information processing system that operates in said second power mode into said first power mode if the number of ready state application tasks exceeds a predetermined value when said first application task ends a predetermined processing unit.

16. The information processing system according to claim 13,

wherein said operating system starts up said ready state watching task that manages the number of ready state application tasks and enables said processor to execute said ready state watching task for each of said plurality of processing units, thereby managing the number of ready state application tasks.

17. An operating system for controlling an information processing system that includes a processor and a timer,

wherein said system includes a system call for outputting the number of ready state application tasks; and

wherein said system enables said information processing system to raise both of the clock frequency and the source voltage if there is any application task set in said ready state other than an object application task to be executed and lower both of said clock frequency and said

source voltage if there is no such ready state application task.